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09/211,677	12/14/1998	HYUN CHANG LEE	8733D-7153	9588

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EXAMINER	
NGUYEN, KEVIN M	

ART UNIT	PAPER NUMBER
2674	39

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/211,677	Applicant(s) LEE, HYUN CHANG	
	Examiner Kevin M. Nguyen	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-37 and 56-88* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-37 and 56-88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/14/1998* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/13/2004 has been entered. An action on the RCE follows:

Drawings

2. Figures 11A and 13 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 27-37 and 56-88 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al (US 5,587,722).

As to claim 27, Suzuki et al teaches an active matrix liquid crystal display apparatus associated with a method, the apparatus comprising:

[recited in lines 2-5 and 10-12 of claim 27]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

[recited in lines 6-9 of claim 27]

In the potential dividing resistances R1 and R2, one end is connected to the power supply VVDD (a first voltage source as claimed) and the other end is connected to the side of the ground (a reference as claimed) through a switching transistor 14 (a switch as claimed, col. 5, lines 36-41).

As the control voltage VCKX becomes the high level, the switching transistor 14 is in the on-state, so that the level of the supply voltage supplied to the shift register 3 is reduced, for example, from the VVDD set at 13.5 V (a first voltage as claimed) to the about 8.5 V (a second voltage as claimed) (col. 6, lines 10-15).

[recited in lines 13-16 of claim 27]

wherein gate pulses GP are applied to a gate electrode of each transistor during a selected period of time for writing video signals Vsig to each pixel, and the applying of the gate pulses GP is stopped in a non-selected period of time for holding the written video signals Vsig, thereby performing the video display (col. 3, lines 20-25).

[recited in lines 17-22 of claim 27]

According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called IH-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30).

[recited in lines 23-26 of claim 27]

In the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals Vsig is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level Vgate1 of the gate pulses GP to be the value of Vgate2 directly before a transition from the selected period of time to the non-selected period of time (col. 3,lines 52-57).

there is generated a large potential difference between the gate voltage Vgate1 and the video signals Vsig. By dropping the gate pulses after lowering the gate voltage Vgate1 to the value of Vgate2 once, it is possible to make the potential difference small between the gate line and the source electrode at the transition from the selected period

of time to the non-selected period of time. This makes it possible to effectively suppress the voltage shift ΔV (col. 3, line 65 to col. 4, line 6).

As to claims 56, 62, Suzuki et al teaches an active matrix liquid crystal display device associated with a method, the apparatus comprising:

[recited in lines 2-7 of claim 56]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

a clock driver (a scanning clock signal as claimed) for supplying clock pulses Vck1 and Vck2 and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

[recited in lines 8-13 of claim 56]

According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called IH-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30).

As described above, it is possible to suppress the voltage shift of the video signals by shaping a fall of the gate pulses smoothly or step-wisely (col. 6, lines 31-33).

As to claims 71 and 76, Suzuki et al teaches an active matrix liquid crystal display device associated with a method, the apparatus comprising:

[recited in lines 2-12 of claim 71]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

a clock driver (a timing controller as claimed) for supplying clock pulses Vck1 and Vck2 and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

[recited in lines 13-22 of claim 71]

According to a variation in the supply voltage, for example, the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely. During this period of time, in the video signals Vsig, the polarity is alternately inverted for the potential Vcom of the opposed electrode for each horizontal period. The so-called IH-inversion drive is carried out. By such an action, the vertical scanning circuit can suppress the voltage shift of the video signals Vsig written in each pixel by shaping a fall of the gate pulses GP through dropping the gate pulses after lowering the voltage level of the gate pulses GP once directly before stopping the applying of the gate pulses GP (col. 6, lines 16-30).

As described above, it is possible to suppress the voltage shift of the video signals by shaping a fall of the gate pulses smoothly or step-wisely (col. 6, lines 31-33).

As to claims 28-32, 57-61, 63, 77-80, Suzuki et al teaches in the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals Vsig is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level Vgate1 of the gate pulses GP to be the value of Vgate2 directly before a transition from the selected period of time to the non-selected period of time (col. 3,lines 52-57).

the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely (col. 6,lines 16-21).

As to claims 33, Suzuki et al teaches a clock driver (a timing controller as claimed) for supplying clock pulses Vck1 and Vck2 and the like are provided outside the substrate of the active matrix liquid display device (col. 5, lines 54-56).

As to claims 36, Suzuki et al teaches wherein gate pulses GP are applied to a gate electrode of each transistor during a selected period of time for writing video signals Vsig to each pixel, and the applying of the gate pulses GP is stopped in a non-selected period of time for holding the written video signals Vsig, thereby performing the video display (col. 3, lines 20-25).

As to claims 37, 67, Suzuki et al teaches a central point between a pair of potential dividing resistance R1 and R2 (a second voltage source as claimed, col. 5,

lines 34-35) and the other end is connected to the side of the ground (col. 5, lines 36-38).

As to claims 34, 64, Suzuki et al teaches a vertical scanning circuit 1, a gate driver comprising a shift register 3 (fig. 2, col. 5, lines 49-50).

As to claims 65, 68-70, 72-75, 81, Suzuki et al teaches

Recited at col. 5, lines 39-47,

A gate electrode of the switching transistor 14 is periodically applied with a control voltage VCKX. When the switching transistor 14 is in the off-state, the supply voltage is supplied to a shift register 3 as it is, and the voltage level of each gate pulse GP is equal to the supply voltage. On the other hand, when the switching transistor 14 is in the on-state, the voltage divided with the ratio R1/R2 is supplied to the shift register 3, and thereby the voltage level of the gate pulse GP is reduced

Recited at col. 6, lines 10-15,

As the control voltage VCKX becomes the high level, the switching transistor 14 is in the on-state, so that the level of the supply voltage supplied to the shift register 3 is reduced, for example, from the VVDD set at 13.5 V (a first voltage as claimed) to the about 8.5 V (a second voltage as claimed).

Recited at col. 3, lines 52-57,

In the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals Vsig is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level Vgate1 of the gate pulses GP to be the

value of Vgate2 directly before a transition from the selected period of time to the non-selected period of time.

As to claim 82, Suzuki et al teaches an active matrix liquid crystal display device comprising:

[recited in lines 2-9 and 14-15 of claim 82]

Referring to fig. 3, a pixel LP, a switching transistor Tr, a video signal Vsig, a gate pulse GP, a data driver 2, a scanning driver 1 (col. 4, lines 40-53).

[recited in lines 8-13 of claim 82]

In the potential dividing resistances R1 and R2, one end is connected to the power supply VVDD (a first voltage source as claimed) and the other end is connected to the side of the ground through a switching transistor 14 (col. 5, lines 36-41).

a central point between a pair of potential dividing resistance R1 and R2 (a second voltage source as claimed, col. 5, lines 34-35)

As the control voltage VCKX becomes the high level, the switching transistor 14 is in the on-state, so that the level of the supply voltage supplied to the shift register 3 is reduced, for example, from the VVDD set at 13.5 V (a first voltage as claimed) to the about 8.5 V (a second voltage as claimed) (col. 6, lines 10-15).

As to claims 83, 84, Suzuki et al teaches in the means as shown in FIG. 1B, the voltage shift ΔV of the written video signals Vsig is suppressed by shaping a fall of the gate pulses through dropping the gate pulses after lowering the voltage level Vgate1 of the gate pulses GP to be the value of Vgate2 directly before a transition from the selected period of time to the non-selected period of time (col. 3,lines 52-57).

the n-th gate pulse GP (n) is changed in level step-wisely from 13.5 V to 8.5 V within one horizontal period. The gate pulse GP (n+1) corresponding to the (n+1)-th gate line is generated within the next horizontal period, and which is changed in level step-wisely (col. 6,lines 16-21).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 35, 85, 86 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al in view of Applicant's Admitted Prior Art hereinafter AAPA.

As to claims 35, 85, 86, Suzuki et al teaches all of the claimed limitations, except for the gate signal line includes a distributed series resistance and a distributed capacitance.

However, AAPA discloses the gate signal line includes a distributed series resistance R1 and a distributed capacitance C1 (see figure 3, page 5, lines 2-5). Since a waveform modifying circuit such as an integrator for each gate line must be added (page 5, lines 30-32).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify each Suzuki's gate signal line including a distributed series resistance R1 and a distributed capacitance C1, in view of the disclosing AAPA

because this would eliminate flickering and residual image (see page 5, lines 29-30 of AAPA).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kevin M. Nguyen** whose telephone number is **703-305-6209**. The examiner can normally be reached on MON-THU from 9:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Richard A Hjerpe** can be reached on **703-305-4709**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KN
June 17, 2004

XIAO WU
PRIMARY EXAMINER